PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BOARD OF PATENT APPEALS AND INTERFERENCES

In Re Application of : Gengying Gao

Serial No.: 09/670,154 Examiner: Trung Q. Nguyen

Filed: 9/26/2000 Art Unit: 2829

For: METHOD OF TESTING THE ELECTROSTATIC DISCHARGE PERFORMANCE OF AN IC DEVICE

SUPPLEMENTAL APPEAL BRIEF
IN SUPPORT OF APPELLANTS' APPEAL
TO THE BOARD OF PATENT APPEALS AND INTERFERENCES

Hon. Commissioner of
Patents and Trademarks
Washington, DC 20231

Dear Sir:

The Appellants hereby submit this Supplemental Brief in triplicate in support of their request for reinstatement of the appeal after the examiner sought to reopen prosecution by way of Office action mailed August 13, 2003, after an Appeal Brief had been file. The Appellants respectfully request consideration of this appeal by the Board of Patent Appeals and Interferences for allowance of the above patent application.

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I. REAL PARTY IN INTEREST

The real party in interest is National Semiconductor Corporation, a corporation of Delaware having a principle place of business at 2900 Semiconductor Drive, M/S D3-579, Santa Clara, CA 95051

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences

III. STATUS OF THE CLAIMS

Claims 1 to 20 are currently pending. No claims have been cancelled or added. Claims 1 to 20 stand rejected by the Examiner under the Final Rejection mailed December 18, 2002 and after the non-final rejection mailed 8/13/2003.

Claims 1 to 20 stand rejected under 35 U.S.C. § 112, and under 35 U.S.C. § 102 as being unpatentable over Paniccia et al (US 5,872,360) and are being appealed.

IV. STATUS OF AMENDMENTS

Amendments to claims 1 and 8 were filed after the final rejection and were initially not entered on the premise that they would not place the application in a better form for appeal. However, the examiner subsequently reopened prosecution and thus the amendments stand as entered.

V. SUMMARY OF INVENTION

The invention deals with a new method of testing the resilience of an integrated circuit device to electrostatic discharge (ESD). In the past ESD resilience

involved a destructive approach involving discharging charge into the pins of the IC device. In contrast, the present invention provides a way of determining the ESD resilience in a non-destructive manner using a laser beam, and making a determination based on the amount of light reflected by the diffusion region of the IC compared to the amount of light absorbed by the diffusion region. This is described in the first paragraph of the Summary of the Invention (page 1, lines 22-24), page 3, lines 13-17, and page 4 lines 23-31 read with Figure 3.

Testing of ESD resilience has nothing to do with debugging a chip to determine whether it has defects. In fact, the chip may very well work fine but simply have a low ability to handle electrostatic discharges. It is a chip's ability to handle ESD that the present invention addresses, and it manages to do this in a non-destructive manner.

VI. ISSUES

The issues are whether the specification provides support for good ESD performance, and whether references dealing with the debugging of a chip or IC can be used in rejecting claims directed to a method of detecting resilience of a chip to ESD events.

Also, the question remains whether an explicit limitation in a claim dealing with a comparison of the light reflection results from a tested chip with light reflection results from a chip with known ESD resilience, can simply be ignored.

VII. GROUPING OF CLAIMS

Claims 1-20 were rejected based on the common argument that Paniccia et al anticipated each of the claims. Claim 1 is the only independent claim, with claims 2-20 depending from it.

VIII. ARGUMENT

Claim rejections - 35 USC 112

Claim 27 was rejected under 35 USC 112 as containing subject matter which is not described in the specification.

It is respectfully pointed out that there is no claim 27 in the application.

Claim 1 was rejected on the basis that the specification and drawings do not support good ESD performance, and that it is unclear what the characteristics of good ESD performance were.

It is respectfully pointed out that ESD (Electrostatic Discharge) is a term commonly used in the art of electronic devices and protection of electronic devices. The high current associated with an ESD event can cause damage to electronic circuit elements by exceeding the current handling capabilities of the circuit elements. This is common knowledge in the art, hence ESD protection devices are employed to shunt ESD current to ground, or alternatively the devices are made self-protecting by making them more robust to be able to withstand the high ESD currents. This invention deals with the latter situation and provides a way of testing the resilience of the devices to ESD events. In fact, the Discussion of the Prior Art section of the present application discusses the issue of ESD resilience and the destructive nature of prior art ESD testing techniques.

The examiner also argues that it is well known to all those skilled in the art to use a laser beam to test the ESD.

The examiner, however, fails to disclose a single reference in support of this contention except for citing Paniccia, which misstates what Paniccia stands for, as is discussed in more detail below in response to the examiner's 35 USC 102 rejection.

The examiner also argues that the drawing and specification do not give any support for I/O cells.

It is respectfully pointed out that page 4, lines 10-25 deal in detail with I/O cells since I/O cells are the circuit elements typically exposed to ESD events.

Claim rejections - 35 USC 102

Claims 1-20 were rejected under 35 USC 102(b) over Paniccia.

It is respectfully submitted that Paniccia does not disclose testing ESD performance. As discussed in response to the previous Office actions and in the original Appeal Brief, (lines 103-110 on page 5), Paniccia does not deal with testing of ESD resilience, and in fact nowhere states or suggests that it does so. Paniccia, instead, discusses the problems of debugging a new product (col. 1, lines 53-57). It then proposes a solution for determining voltage applied to a p-n junction by monitoring the electric field by monitoring the electro-absorption of a mode-locked laser (col. 7,lines 18-23).

Nowhere does Paniccia describe or suggest ways of monitoring ESD performance of an IC device.

Claim 1, in contrast, specifically defines a method of monitoring ESD performance. This is not a feature proposed in arguments or only in the specification, but is specifically mentioned in claim 1.

However, in order to further distinguish the present invention from Paniccia, claim 1 was amended to include the step of comparing the amount of reflected light to the amount of reflected light from an I/O cell having good ESD performance (see page 4, lines 23-31). This step also not present in Paniccia and is not suggested anywhere in Paniccia.

Since the remaining claims 2-20 depend from claim 1, they will include the new limitation, and are therefore also distinguishable over Paniccia.

As to claim 8, it is respectfully submitted that Paniccia does not mention averaging a number of measurements. Nevertheless, claim 8 was amended to specify that the samples are taken at the same I/O signal voltage level. This

further distinguishes from Paniccia, which clearly discusses measurements at different electric fields and temperatures (Fig. 7 and col. 7, lines 7-17).

As to claim 15, it is respectfully submitted that Paniccia does not discuss any testing in pre-packaged form. The section referred to by the examiner (col. 5, lines 50-55) has to be read in the context of the rest of the sentence which clearly states that it is often necessary to do the testing while the chip is packaged. In other words the section specifically sets the context of the problem, namely testing a packaged device. This is used by Paniccia to justify the need for a laser. Nowhere does it mention or contemplate testing of unfinished devices.

As to claim 16, it is respectfully submitted that Paniccia does not disclose that the device includes only some of its layers. The section referred to by the examiner (col. 1, lines 62-67) merely states that a typical IC has multiple layers and that it is therefore difficult to access nodes buried deep in the chip. There is no mention of testing while there are only some of the layers formed.

Response to specific arguments raised by examiner

The examiner argued that ESD testing using a laser beam is known to all those skilled in the art. This is entirely unsupported by any fact since there is no cited reference to support this contention. Furthermore, claim 1 specifically includes the limitation of comparing to an I/O cell having good ESD performance. This is not disclosed or suggested in Paniccia or any other IC testing references.

The examiner argued that Paniccia discloses testing a device with only some of its layers and that it disclosed using a continuous wave laser to probe the IC

device. As has been discussed above, Paniccia does not disclose a device having only some of its layers (see arguments above).

It is unclear what the examiner's argument is regarding the use in Paniccia of a continuous wave laser. In fact Paniccia specifically refers to using a mode-locked laser. Fig 7 and col. 8, lines 6-15 of Paniccia specify a mode-locked laser, not a continuous wave laser. In any event the present application uses the continuous wave laser simply as one way of positioning the mode-locked laser. Paniccia does not disclose using a continuous wave laser as a positioning means or for any other purpose for that matter.

In any event, all of the dependent claims depend from claim 1 and therefore include the limitations of claim 1, and are therefore, by that reason alone, distinguishable over the prior art.

The examiner states that any special structural or functional aspects of the Applicant's invention have to be clear from the claims themselves, and goes on to state various case law. The examiner's arguments, while correct, do not bear on the present facts where the limitations are specifically recited in the claims. The claims themselves include the limitation of testing ESD performance and also include the limitation of comparing reflected light to the light reflected from an I/O cell with good ESD performance. Each of these limitations explicitly distinguish over the cited art.

In view of the fact that claim 1 specifically deals with testing of ESD performance and is further amended to specifically include the limitation of comparing the light reflected to the light reflected from an I/O cell with good ESD performance, it is respectfully submitted that all of the claims are distinguishable over the prior art. Furthermore, claims 10, 15, 16, 18 add additional limitations not disclosed in

Paniccia.

Allowance of all of the claims is therefore respectfully requested.

Charge Our Deposit Account

If there are any further charges not accounted for herein, please charge them to our deposit account No. 140448

Respectfully submitted,

Vollrath & Associates

Date: 11/11/, 2003

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IX. APPENDIX

1. A method of testing the ESD performance of an IC device, comprising probing the device with a laser beam, monitoring the amount of light reflected from the device, and comparing the amount of light reflected to the amount of light reflected from an I/O cell having good ESD performance.

2. A method of Claim 1, wherein the laser beam is used to probe the IC device.

3. A method of Claim 2, wherein the energy of the laser beam corresponds substantially to the bandgap of the substrate of the device.

4. A method of Claim 3, wherein the substrate is silicon and the energy of the laser beam is about 1.1eV.

5. A method of claim 3, wherein the diffusions of the IC device are probed with the laser beam.

6. A method of Claim 5, wherein in the device is probed through the back of the device.

7. A method of Claim 6, wherein the diffusions of I/O cells are probed to determine how much light is absorbed and how much light is reflected by the diffusions.

8. A method of Claim 5, wherein several samples are taken of each probed location, at the same I/O signal voltage level, and the results averaged.

9. A method of Claim 1, wherein a mode-locked laser is used to probe the IC device.

10. A method of Claim 9, wherein a continuous wave laser is used in addition to the mode-locked laser, to provide an image of the IC device in order to facilitate the positioning of the beam of the mode-locked laser.

11. A method of Claim 9, wherein the mode-locked laser is positioned by a user.

12. A method of Claim 9, wherein the mode-locked laser is positioned automatically using image recognition.

13. A method of Claim 5, wherein power is supplied to the device during testing.

14. A method of Claim 13, wherein the testing is performed on the device in a packaged form.

15. A method of Claim 13, wherein the testing is performed on the device in a prepackaged form.

16. A method of Claim 15, wherein the device includes only some of its layers.

17. A method of Claim 6, wherein a mode-locked laser is used to probe the IC device.

18. A method of Claim 17, wherein a continuous wave laser is used in addition to the mode-locked laser, to provide an image of the IC device in order to facilitate the positioning of the beam of the mode-locked laser.

19. A method of Claim 17, wherein the mode-locked laser is positioned by a user.

20. A method of Claim 17, wherein the mode-locked laser is positioned automatically using image recognition.